A Two-Stage Monolithic IF Amplifier Utilizing a High Dielectric Constant Capacitor *

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Abstract

A two-stage monolithic IF amplifier incorporating sputtered Ta_2O_5 capacitor has been fabricated. The monolithic capacitor is based on a composite layer structure consisting of Au, Ta, Ta_2O_5, Ta and Au. This layered structure is sequentially deposited in a single sputtering run, which eliminates all possibility of particulate contamination. As a result a thin pinhole-free dielectric layer can be deposited over large areas, and 140 pF capacitors have been fabricated with excellent yields. The large unit area capacitance of 1500 pF/mm^2 available with the present process has the potential for reducing the size and cost of both microwave monolithic circuits and hybrid thin-film circuits.

The monolithic amplifiers exhibit a gain of 17.5 ±1.0 dB from 1.2 to 2.6 GHz and a minimum noise figure of ~2.7 dB with an associated gain of 17.5 dB at 1.7 GHz.

Capacitors for Microwave Monolithic Circuits

A monolithic IF amplifier has been fabricated for use in a millimeter-wave heterodyne receiver chip[1]. The IF frequency range of the receiver goes from 1.2 to 2.8 GHz, which is determined by the bandwidth of the balanced mixer. The design of multistage amplifiers in this frequency range requires interstage coupling capacitors from 40 to 80 pF. This requirement imposes a difficult fabrication problem because capacitors based on dielectric materials presently used in monolithic fabrication can achieve only modest values of capacitances per unit area. Typical values of unit area capacitances obtained in the present work using 5000 Å of polyimide, SiO_2 or Si_3N_4 are 53, 70, and 132 pF/mm^2, respectively, as shown in Table I. Use of these low dielectric constant materials for the fabrication of 60 pF interstage coupling capacitors resulted in low yield because of the high probability of including pinholes in the large areas required. A solution to this problem is the use of a higher dielectric constant material, such as Ta_2O_5.

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Anodized Ta_2O_5 capacitors with Ta anodes are utilized in silicon ICs. Unit area capacitances in the range of 600 pF/mm^2 have been obtained[2], but high conductor losses in the Ta electrode limit their operation to frequencies below 10 kHz. Incorporation of an Al layer beneath the dielectric has increased the operating frequency to 10 MHz[2]. Although further improvements seem possible, the anodized Ta_2O_5 capacitor process using an Al underlayer is not compatible with Au-based metallization systems used in GaAs monolithic circuits.

In view of these limitations we have developed a reactively sputtered Ta_2O_5 thin-film capacitor process that is compatible with monolithic integration of GaAs circuits and capable of achieving unit area capacitances of 1500 pF/mm^2. This value is over an order of magnitude higher than the unit area capacitances that are obtained from Si_3N_4, SiO_2 and polyimide capacitors.

High Frequency Ta_2O_5 Capacitors

The Ta_2O_5 dielectric layer for use in the capacitor can be obtained by anodic oxidation[3] or thermal oxidation[4] of a Ta layer. Alternatively, Ta_2O_5 can be reactively sputtered[5,6] from a Ta target by Ar ions in the presence of partial pressures of oxygen. Auger analysis reveals that the chemical composition of the layers obtained by the three techniques are essentially the same[7]. Typical values of capacitances per unit area obtained from capacitors of each type are shown in Table I.

A photograph of a high frequency Ta_2O_5 capacitor is shown in Fig. 1. The top electrode measures 125 μm by 125 μm. The cross section of the capacitor shown below reveals a sequence of five layers: Au, Ta, Ta_2O_5, Ta, and Au. The Au layers are the top and bottom electrodes for the capacitor, the Ta_2O_5 layer is the dielectric and the thin Ta layers serve the purpose of bonding the Ta_2O_5 to the Au. Without the Ta layer, adhesion of Ta_2O_5 to the Au would be poor. Thicknesses of the layers are 1250 Å, 250 Å, and 1750 Å for Au, Ta, and Ta_2O_5, respectively. To minimize losses, the thicknesses of the Ta layer should be kept to the minimum required for good adhesion.

In the reactively sputtered capacitor process the Au, Ta, Ta_2O_5, Ta, and Au layers are deposited

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sequentially in a single sputtering run without breaking vacuum. An important difference between this process and the oxidation processes is that wafer handling does not occur at the formation of the dielectric layer, so that the susceptibility to particulate contamination is greatly reduced. The apparatus used for the deposition of the composite layer is a RANDEX parallel-plate RF diode sputtering unit, as shown in Fig. 2. The Au and Ta layers are deposited from their respective targets in an Ar plasma at 50 W RF power. The flow rate of Ar is 20 sccm. Deposition of the Ta_2O_5 layer is accomplished by reactive sputtering the Ta target using a mixture of O_2 and Ar. The RF power is maintained at 50 W and the ratio of O_2 to Ar flow rate is 15%. The deposition rate of the Ta_2O_5 layer is 13 Å/min compared to a rate of 50 Å/min for Ta. The reduced rate is the result of the formation of an oxide layer on the Ta target, which is then sputter-deposited by the Ar ions onto the substrate at a slower rate. The remaining Ta and Au layers are deposited under conditions described previously. Layer thicknesses for the Au, Ta and Ta_2O_5 are 1250 Å, 250 Å and 1750 Å, respectively, and the respective deposition times were 6 min, 5 min and 135 min.

Fabrication Sequence of Two-Stage Amplifier

The fabrication sequence of the two-stage amplifier uses 9 mask levels, of which 3 levels are associated with the fabrication of the capacitor, 3 levels are used for the fabrication of FETs and the remaining 3 levels are for the fabrication of transmission lines and bias lines. Figure 3 shows a diagram of this fabrication process. Wafer processing begins with the formation of the source and drain ohmic contacts of the FETs. In step #2 individual devices are isolated electrically by means of mesa etching. In step #3 the composite layers for the capacitor are sputter-deposited and defined using a lift-off process. In step #4 the top Au layer is defined by wet etching and the underlying Ta layer by plasma etching. Although it was not implemented in the present case, trimming of capacitances could be incorporated into the process at this step. In step #5 access to the bottom electrode of the capacitor is provided by etching the Ta_2O_5/Ta layers with a CF_4 plasma in a barrel type reactor. Etching was performed at a power level of 150 W and at a pressure of 2 Torr. In step #6 a polyimide layer is defined to provide support for the connection to the top electrode of the capacitor. In step #7 the FET gates are formed by a lift-off process. The gate metal, which is based on a Au metallization system, serves several functions in the remainder of the fabrication. It is used as a plating base for transmission lines and connections to the capacitors, and in step #9 portions of gate metal in the field are protected during etching to leave bias lines on the circuit while unwanted areas are removed. Plating of transmission lines and bonding pads takes place in step #8.

Two-Stage IF Amplifier with Ta_2O_5 Interstage Coupling Capacitor.

The reactively sputtered Ta_2O_5 capacitor described previously was integrated in the two-stage monolithic IF amplifier shown in Fig. 4. The capacitance was 140 pF and the area of the capacitor was 9.78×10^{-2} mm^2. This capacitance is about twice the desired value because the mask set was designed assuming a lower value of capacitance per unit area. The chip measures 2.5 mm by 5.0 mm. Input matching of the first stage amplifier is provided by a pair of open-circuited 8 Ω stubs followed by a 140 Ω high-impedance line. Electrical lengths of the stub and transmission line at 2 GHz are 4.3° and 35.3°, respectively. The FETs have 1 μm by 500 μm gates positioned in a drain-to-source spacing of 5 μm. The epitaxial layer is directly implanted with Se^+ ions into an undoped GaAs semi-insulating substrate. Bias lines for the drains and the gate of the second stage are also indicated on the photograph. The interstage matching network, is identical to the input matching network with the exception of the electrical length of the open-circuited stub, which is 8.6° at 2 GHz.

Electrical Test Results

Electrical evaluation of the reactively sputtered capacitors was performed with a 1 MHz capacitance bridge and with a network analyzer. Figure 5 shows a comparison of the 1 MHz data with the network analyzer data obtained from the capacitor connected in shunt between two sections of microstrip lines. Agreement of the data is good to approximately 300 MHz. Values of the discrete capacitor and loss tangent are ~24 pF and ~0.03 respectively. Divergence of the data at 1 GHz is an artifact of the resonance between the capacitor and the inductance associated with the bonding wire used to connect the capacitor to the microstriplines and to ground. Evaluation of the capacitor as an interstage coupling capacitor was performed on a 140 pF capacitor, which was cut out from a actual monolithic two-stage amplifier. Test results show an insertion loss less than 0.15 dB in the frequency band of interest.

The monolithic amplifiers were mounted in suitable fixtures and measured using a network analyzer. The noise figure circles at 1.7 GHz are shown in Fig. 6 and indicate a minimum noise figure of 2.5 dB. When the amplifier is connected to a 50 Ω source, the noise figure is 2.7 dB at 1.7 GHz, of which 1 dB is the contribution of losses in the high impedance line. The associated gain is 17.5 dB. The bandwidth of the IF amplifier is shown in Fig. 7. The unit exhibits a gain in excess of 16.5 dB from 1.0 to 2.8 GHz.

Discussion and Summary

Integration of the two-stage amplifier in the 31 GHz heterodyne receiver should provide an overall conversion gain above 10 dB. The 17.5 dB

gain of the IF amplifier is sufficient to suppress noise contributions from additional stages, establishing the single-sideband receiver noise figure in the range of 9 to 10 dB.

Losses in the capacitor arise primarily from RF losses in the electrodes, rather than in the dielectric material. Therefore, higher Q's can be achieved by increasing the thickness of the electrodes and reducing the area of capacitors to produce capacitances consistent with circuit design requirements and safe fabrication limits. In the present application the Au layers can be increased to ~2000 Å and the area of the interstage coupling capacitor can be reduced by 50% and still achieve an adequate series reactance.

The reactively sputtered Ta_2O_5 capacitor, in addition to being necessary for the two-stage monolithic IF amplifier, may be useful for other monolithic circuits because large capacitances can be achieved with small size and high fabrication yield. Since coupling and bypass capacitors occupy a considerable fraction of the area in most microwave monolithic circuits, the large unit-area capacitance of the present capacitor can reduce the size and cost of both monolithic as well as thin-film hybrid circuits.

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MATERIAL	RELATIVE DIELECTRIC CONSTANT	THICKNESS (Å)	CAPACITANCE (pF/mm^2)
POLYIMIDE	3	5000	53
SiO_2	4-5	5000	71
Si_3N_4	6-8	5000	132
ANODIZED Ta_2O_5	~27-30	~3000	834
THERMALLY OXIDIZED Ta_2O_5	~27-30	~2000	1251
REACTIVELY SPUTTERED Ta_2O_5	~27-30	~1750	1430

Table I. Comparison of dielectric materials for thin film capacitors.

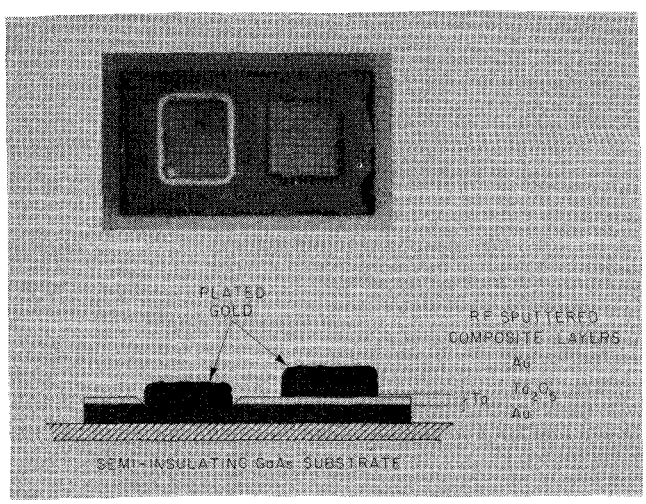

Figure 1. High frequency tantalum pentoxide capacitor.